# SKYPER 32PRO R ...

**SKYPER™**

## IGBT Driver Core

**SKYPER 32PRO R**

Preliminary Data

### Features

- Two output channels
- Integrated potential free power supply
- Under voltage protection
- Drive interlock top / bottom
- Dynamic short circuit protection
- Halt logic signal
- Failure management
- Soft turn-off
- External error input (sec. side)
- IEC 60068-1 (climate) 40/085/56, no condensation and no dripping water permitted, non-corrosive, climate class 3K3 acc. EN60721
- Coated with varnish

### Typical Applications

- Driver for IGBT modules in bridge circuits in choppers, inverter drives, UPS and welding inverters
- DC bus voltage up to 1200V

1) with external high voltage diode
2) Please Note: the isolation test is not performed as a series test at SEMIKRON and must be performed by the user
3) accroding to VDE 0110-20

Isolation coordination in compliance with EN50178 PD2

Operating temperature is real ambient temperature around the driver core

Degree of protection: IP00

**Absolute Maximum Ratings**

| Symbol | Conditions | Values | Units |
|---|---|---|---|
| $V_S$ | Supply voltage primary | 16 | V |
| $V_{iH}$ | Input signal voltage (High) | $V_S$ + 0,3 | V |
| $V_{iL}$ | Input signal voltage (Low) | GND - 0,3 | V |
| $Iout_{PEAK}$ | Output peak current | 15 | A |
| $Iout_{AVmax}$ | Output average current | 50 | mA |
| $f_{max}$ | max. switching frequency | 50 | kHz |
| $V_{CE}$ | Collector emitter voltage sense across the IGBT 1) | 1700 | V |
| dv/dt | Rate of rise and fall of voltage secondary to primary side | 50 | kV/µs |
| $V_{isolIO}$ | Isolation test voltage input - output (AC, rms, 2s) 2) | 4000 | V |
| $V_{isolPD}$ | Partial discharge extinction voltage, rms, $Q_{PD} \leq 10pC$ 3) | 1500 | V |
| $V_{isol12}$ | Isolation test voltage output 1 - output 2 (AC, rms, 2s) 2) | 1500 | V |
| $R_{Gonmin}$ | Minimum rating for $R_{Gon}$ | 1,5 | Ω |
| $R_{Goffmin}$ | Minimum rating for $R_{Goff}$ | 1,5 | Ω |
| $Q_{out/pulse}$ | Max. rating for output charge per pulse | 6,3 | µC |
| $T_{op}$ | Operating temperature | - 40 ... + 85 | °C |
| $T_{stg}$ | Storage temperature | - 40 ... + 85 | °C |

**Characteristics** $T_a$ = 25 °C, unless otherwise specified

| Symbol | Conditions | min. | typ. | max. | Units |
|---|---|---|---|---|---|
| $V_S$ | Supply voltage primary side | 14,4 | 15 | 15,6 | V |
| $I_{SO}$ | Supply current primary side (no load) | 80 | | | mA |
| | Supply current primary side (max.) | | | 500 | mA |
| $V_i$ | Input signal voltage on/off | | 15 / 0 | | V |
| $V_{iT+}$ | Input threshold voltage (High) | | | 12,3 | V |
| $V_{iT-}$ | Input threshold voltage (Low) | 4,6 | | | V |
| $R_{in}$ | Input resistance (switching signals, HALT signal) | | 100 | | kΩ |
| $V_{G(on)}$ | Turn on gate voltage output | | + 15 | | V |
| $V_{G(off)}$ | Turn off gate voltage output | | - 7 | | V |
| $f_{ASIC}$ | Asic system switching frequency | | 8 | | MHz |
| $t_{d(on)IO}$ | Input-output turn-on propagation time | | 1,2 | | µs |
| $t_{d(off)IO}$ | Input-output turn-off propagation time | | 1,2 | | µs |
| $t_{d(err)}$ | Error input-output propagation time | 3,1 | | 5,8 | µs |
| $t_{d(err)ext}$ | External error (secondary side) input-output propagation time | | 6,1 | | µs |
| $t_{pERRRESET}$ | Error reset time | | 9 | | µs |
| $t_{TD}$ | Top-Bot Interlock Dead Time | no interlock | | 4,3 | µs |
| $C_{ps}$ | Coupling capacitance primary secondary | | 12 | | pF |
| w | weight | | 34 | | g |
| MTBF | Mean Time Between Failure @ $T_a$=40°C, max. load | | 1,3 | | $10^6$ h |

This technical information specifies semiconductor devices but promises no characteristics. No warranty or guarantee expressed or implied is made regarding delivery, performance or suitability.

## Technical Explanations

Revision 03
Status: ***preliminary***
Prepared by: Markus Hermwille

| *This Technical Explanation is valid for the following parts:* | | *Related Documents:* | |
|---|---|---|---|
| *part number:* | *L6100202* | *title:* | *Data Sheet SKYPER 32PRO R* |
| *date code (YYWW):* | *≥ 0705* | *version:* | *2007-01-19* |

# SKYPER™ 32PRO R

**Content**



**Please note:**
Unless otherwise specified, all values in this technical explanation are typical values. Typical values are the average values expected in large quantities and are provided for information purposes only. These values can and do vary in different applications. All operating parameters should be validated by user's technical experts for each application.

### Application and Handling Instructions

- Please provide for static discharge protection during handling. As long as the hybrid driver is not completely assembled, the input terminals have to be short-circuited. Persons working with devices have to wear a grounded bracelet. Any synthetic floor coverings must not be statically chargeable. Even during transportation the input terminals have to be short-circuited using, for example, conductive rubber. Worktables have to be grounded. The same safety requirements apply to MOSFET- and IGBT-modules.
- Any parasitic inductances within the DC-link have to be minimised. Over-voltages may be absorbed by C- or RCD-snubbers between main terminals for PLUS and MINUS of the power module.
- When first operating a newly developed circuit, SEMIKRON recommends to apply low collector voltage and load current in the beginning and to increase these values gradually, observing the turn-off behaviour of the free-wheeling diode and the turn-off voltage spikes generated across the IGBT. An oscillographic control will be necessary. Additionally, the case temperature of the module has to be monitored. When the circuit works correctly under rated operation conditions, short-circuit testing may be done, starting again with low collector voltage.
- It is important to feed any errors back to the control circuit and to switch off the device immediately in failure events. Repeated turn-on of the IGBT into a short circuit with a high frequency may destroy the device.
- The inputs of the hybrid driver are sensitive to over-voltage. Voltages higher than $V_S$ +0,3V or below -0,3V may destroy these inputs. Therefore, control signal over-voltages exceeding the above values have to be avoided.
- The connecting leads between hybrid driver and the power module should be as short as possible (max. 20cm), the driver leads should be twisted.

### Further application support

Latest information is available at http://www.semikron.com. For design support please read the SEMIKRON Application Manual Power Modules available at http://www.semikron.com.

### General Description

The SKYPER™ 32PRO core constitutes an interface between IGBT modules and the controller. This core is a half bridge driver. Functions for driving, potential separation and protection are integrated in the driver. Thus it can be used to build up a driver solution for IGBT modules.

### Features of SKYPER™ 32PRO

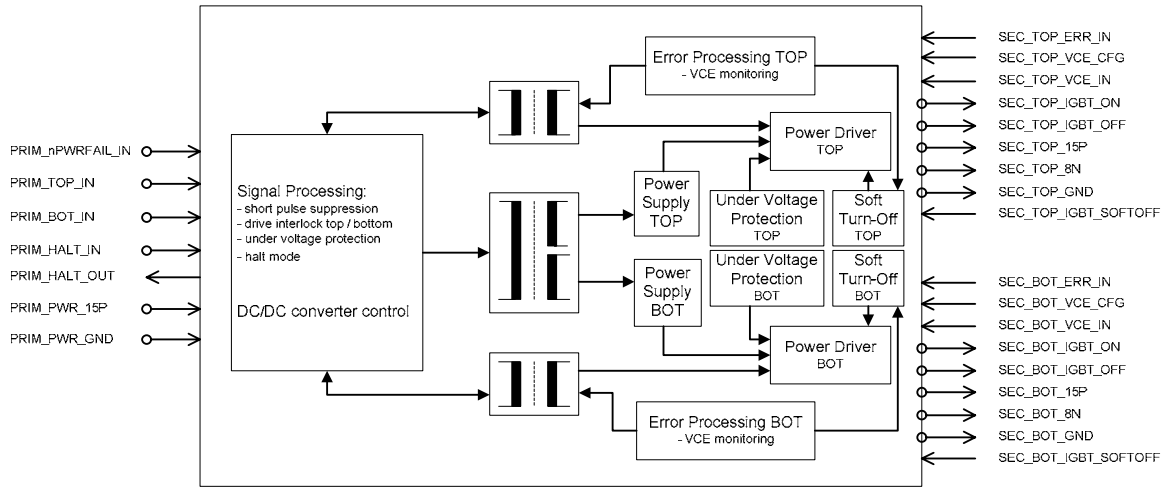
- Two output channels
- Integrated potential free power supply for secondary side
- Short Pulse Suppression (SPS)
- Under Voltage Protection (UVP) primary & secondary
- Under Voltage Reset (UVR)
- Drive interlock (dead time) top / bottom (DT) adjustable
- Dynamic Short Circuit Protection (DSCP) by $V_{CE}$ monitoring and direct switch off
- Soft Turn-Off (STO)
- Halt Logic Signal (HLS)
- Failure Management
- External Error Input
- DC bus voltage up to 1200V
- Coated with varnish

**SKYPER™ 32PRO**

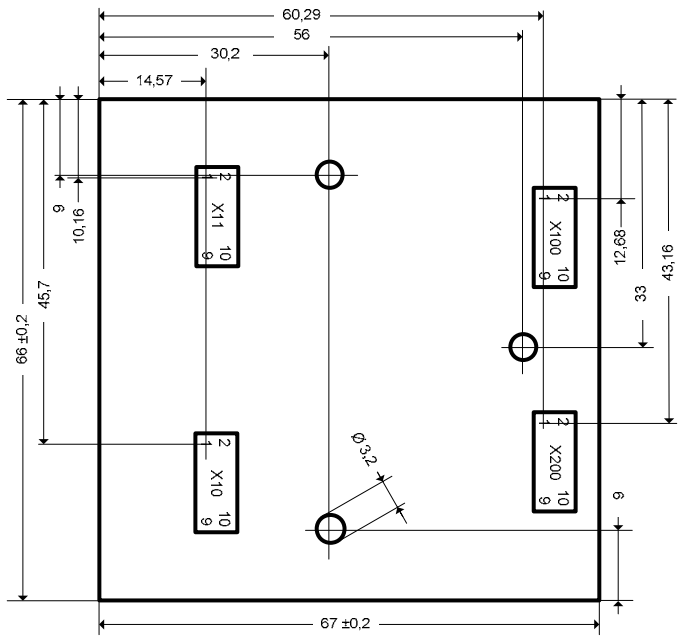
## Block diagram

**Block diagram**



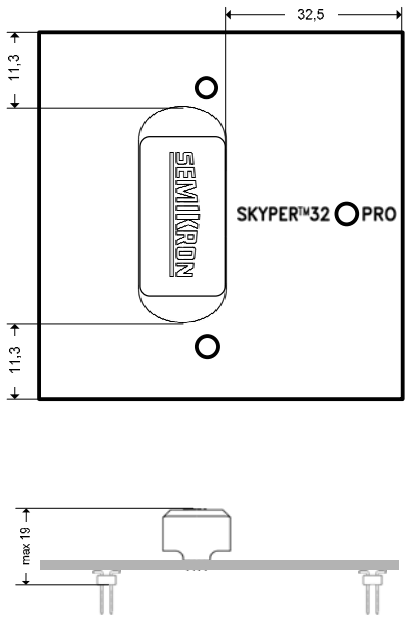

## Dimensions

**Dimensions in mm (bottom view)**



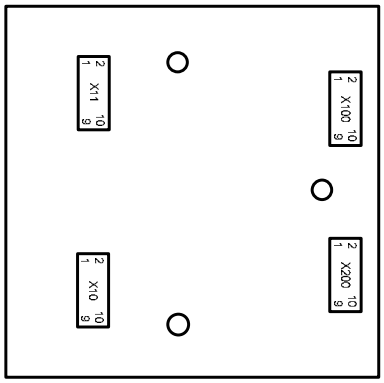
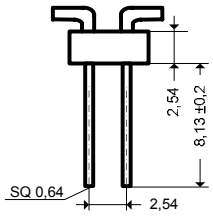

±0,2mm unless otherwise noted

**(top view)**



**PIN Array – Primary Side**

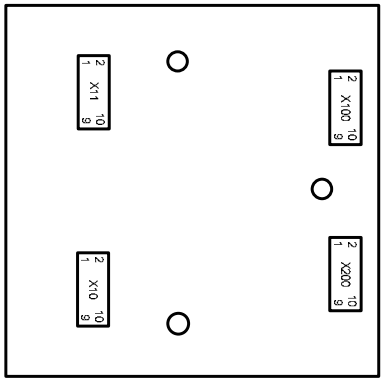
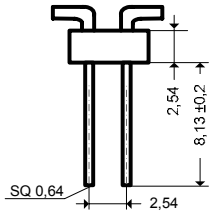
| Connectors | Connector X10 / X11 (RM2,54, 10pin) |
|---|---|
|  |  |



±0,25mm unless otherwise noted

| PIN | Signal | Function | Specification |
|---|---|---|---|
| X10:01 | PRIM_nPWRFAIL_IN | Under Voltage Reset (supervisor reset to be driven by an external circuitry) | Inverted 15 V logic; 100kOhm impedance;<br>LOW = hold;<br>HIGH = normal operation |
| X10:02 | reserved | | |
| X10:03 | PRIM_HALT_OUT | Driver core status output | Digital 15 V logic; max. 2mA;<br>LOW = ready to operate;<br>HIGH = not ready to operate |
| X10:04 | PRIM_HALT_IN | Driver core status input | Digital 15 V logic; 100kOhm impedance;<br>LOW = enable driver;<br>HIGH = disable driver |
| X10:05 | PRIM_PWR_GND | GND for power supply and GND for digital signals | |
| X10:06 | PRIM_PWR_GND | GND for power supply and GND for digital signals | |
| X10:07 | PRIM_TOP_IN | Switching signal input (TOP switch) | Digital 15 V logic; 100kOhm impedance;<br>LOW = TOP switch off;<br>HIGH = TOP switch on |
| X10:08 | PRIM_BOT_IN | Switching signal input (BOTTOM switch) | Digital 15 V logic; 100kOhm impedance;<br>LOW = BOT switch off;<br>HIGH = BOT switch on |
| X10:09 | PRIM_PWR_15P | Drive core power supply | Stabilised +15V ±4% |
| X10:10 | PRIM_PWR_15P | Drive core power supply | Stabilised +15V ±4% |
| X11:01 | reserved | | |
| X11:02 | reserved | | |
| X11:03 | PRIM_PWR_GND | GND for power supply and GND for digital signals | |
| X11:04 | PRIM_PWR_GND | GND for power supply and GND for digital signals | |
| X11:05 | PRIM_CFG_TDT2_IN | Digital adjustment of locking time | Dead time bit #2 |
| X11:06 | PRIM_CFG_SELECT_IN | Signal for neutralizing locking function | |
| X11:07 | PRIM_CFG_TDT3_IN | Digital adjustment of locking time | Dead time bit #3 |
| X11:08 | PRIM_CFG_TDT1_IN | Digital adjustment of locking time | Dead time bit #1 |
| X11:09 | PRIM_PWR_GND | GND for power supply and GND for digital signals | |
| X11:10 | PRIM_PWR_GND | GND for power supply and GND for digital signals | |

**PIN Array – Secondary Side**

| Connectors | Connector X100 / X200 (RM2,54, 10pin) |
|---|---|
|  |  |



±0,25mm unless otherwise noted

| PIN | Signal | Function | Specification |
|---|---|---|---|
| X100:01 | SEC_TOP_VCE_CFG | Input reference voltage adjustment | |
| X100:02 | SEC_TOP_VCE_IN | Input $V_{CE}$ monitoring | |
| X100:03 | SEC_TOP_15P | Output power supply | Stabilised +15V / max. 10mA [1)] |
| X100:04 | SEC_TOP_ERR_IN | External error input | Voltage input; 6,6kOhm impedance; LOW = ERROR |
| X100:05 | SEC_TOP_IGBT_ON | Switch on signal TOP IGBT | |
| X100:06 | SEC_TOP_IGBT_OFF | Switch off signal TOP IGBT | |
| X100:07 | SEC_TOP_GND | GND for power supply and GND for digital signals | |
| X100:08 | SEC_TOP_GND | GND for power supply and GND for digital signals | |
| X100:09 | SEC_TOP_IGBT_SOFTOFF | Control input for setting soft turn-off TOP IGBT | |
| X100:10 | SEC_TOP_8N | Output power supply | Stabilised -7V / max. 10mA [1)] |
| X200:01 | SEC_BOT_VCE_CFG | Input reference voltage adjustment | |
| X200:02 | SEC_ BOT_VCE_IN | Input $V_{CE}$ monitoring | |
| X200:03 | SEC_ BOT_15P | Output power supply | Stabilised +15V / max. 10mA [1)] |
| X200:04 | SEC_ BOT_ERR_IN | External error input | Voltage input; 6,6kOhm impedance; LOW = ERROR |
| X200:05 | SEC_ BOT_IGBT_ON | Switch on signal BOT IGBT | |
| X200:06 | SEC_ BOT_IGBT_OFF | Switch off signal BOT IGBT | |
| X200:07 | SEC_ BOT_GND | GND for power supply and GND for digital signals | |
| X200:08 | SEC_ BOT_GND | GND for power supply and GND for digital signals | |
| X200:09 | SEC_BOT_IGBT_SOFTOFF | Control input for setting soft turn-off BOT IGBT | |
| X200:10 | SEC_BOT_8N | Output power supply | Stabilised -7V / max. 10mA [1)] |

[1)] The average output current of the driver will be reduced accordingly.

### Driver Performance

The driver is designed for application with half bridges or single modules and a maximum gate charge per pulse < 6,3µC. The charge necessary to switch the IGBT is mainly depending on the IGBT's chip size, the DC-link voltage and the gate voltage. This correlation is shown in module datasheets. It should, however, be considered that the driver is turned on at +15V and turned off at -7V. Therefore, the gate voltage will change by 22V during each switching procedure. Unfortunately, many datasheets do not show negative gate voltages. In order to determine the required charge, the upper leg of the charge curve may be prolonged to +22V for determination of approximate charge per switch.
The medium output current of the driver is determined by the switching frequency and the gate charge. The maximum switching frequency may be calculated with the shown equations and is limited by the average current of the driver power supply and the power dissipation of driver components.

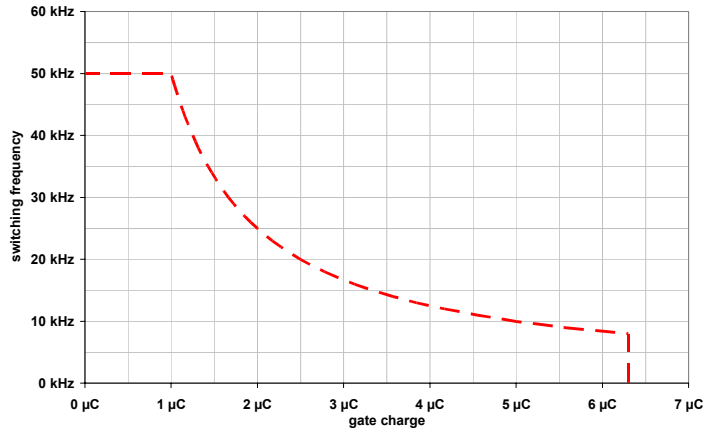
**Calculation Switching Frequency**

$$f_{max} = \frac{Iout_{AVmax}}{Q_{GE}}$$

$f_{max}$: Maximum switching frequency *
$Iout_{AVmax}$: Maximum output average current
$Q_{GE}$: Gate charge of the driven IGBT

*@ $T_{amb}$=25°C

**Maximum Switching Frequency @ different Gate Charges @ $T_{amb}$=25°C**

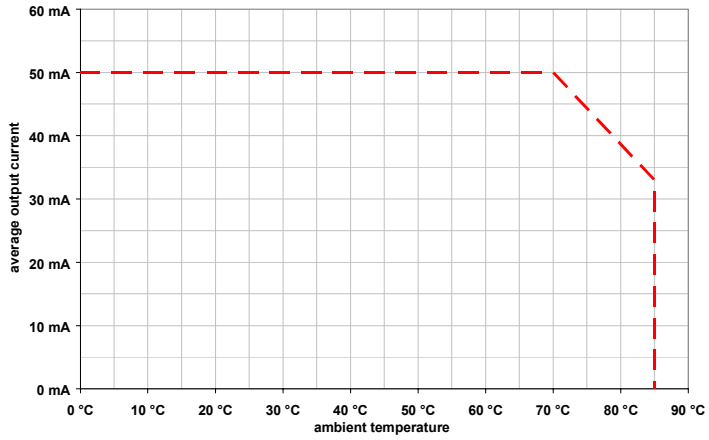



**Calculation Average Output Current**

$$Iout_{AV} = f_{sw} \times Q_{GE}$$

$Iout_{AV}$: Average output current
$f_{sw}$: Switching frequency
$Q_{GE}$: Gate charge of the driven IGBT

**Average Output Current as a Function of the Ambient Temperature**




**Please note:**
The maximum value of the switching frequency is limited to 50kHz due to switching reasons.

### Insulation

Magnetic transformers are used for insulation between gate driver primary and secondary side. The transformer set consists of pulse transformers which are used bidirectional for turn-on and turn-off signals of the IGBT and the error feedback between secondary and primary side, and a DC/DC converter. This converter provides a potential separation (galvanic separation) and power supply for the two secondary (TOP and BOT) sides of the driver. Thus, external transformers for power supply are not required.

| Creepage and Clearance Distance in mm | |
|---|---|
| Primary to secondary | Min. 12,2 |

**Isolation Test Voltage**

The isolation test voltage represents a measure of immunity to transient voltages. The maximum test voltage and time applied once between input and output, and once between output 1 and output 2 are indicated in the absolute maximum ratings. The high-voltage isolation tests and repeated tests of an isolation barrier can degrade isolation capability due to partial discharge. Repeated isolation voltage tests should be performed with reduced voltage. The test voltage must be reduced by 20% for each repeated test.
The isolation of the isolation barrier (transformer) is checked in the part. With exception of the isolation barrier, no active parts, which could break through are used. An isolation test is not performed as a series test. Therefore, the user can perform once the isolation test with voltage and time indicated in the absolute maximum ratings.

**Please note:**
An isolation test is not performed at SEMIKRON as a series test.

**Auxiliary Power Supply**

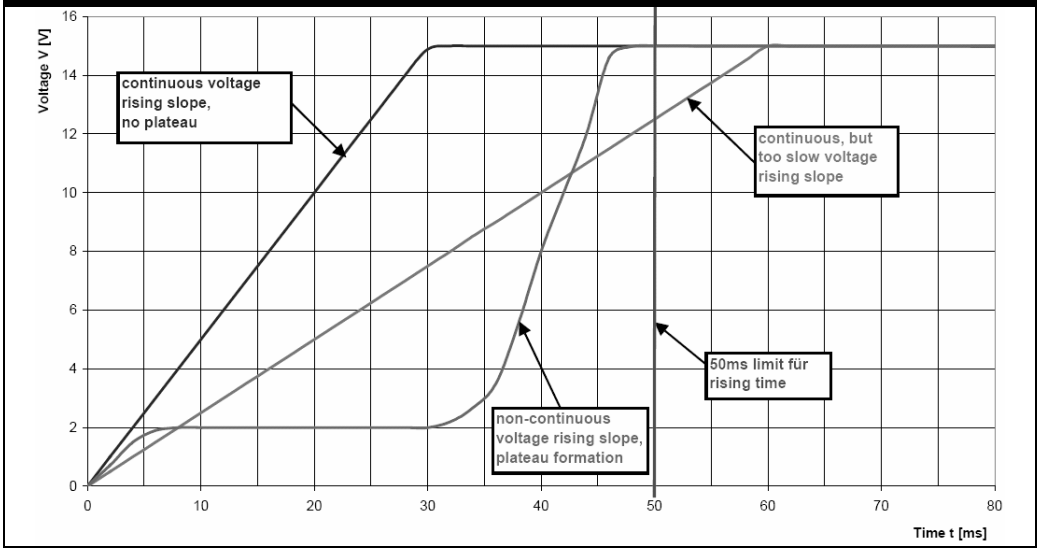
A few basic rules should be followed when dimensioning the customer side power supply for the driver. The following table shows the required features of an appropriate power supply.

| Requirements of the auxiliary power supply | |
|---|---|
| Regulated power supply | +15V ±4% |
| Maximum rise time of auxiliary power supply | 50ms |
| Minimum peak current of auxiliary supply | 1A |
| Power on reset completed after | 150ms |

**Please note:**
Do not apply switching signals during power on reset.

The supplying switched mode power supply may not be turned-off for a short time as consequence of its current limitation. Its output characteristic needs to be considered. Switched mode power supplies with fold-back characteristic or hiccup-mode can create problems if no sufficient over current margin is available. The voltage has to rise continuously and without any plateau formation as shown in the following diagram.

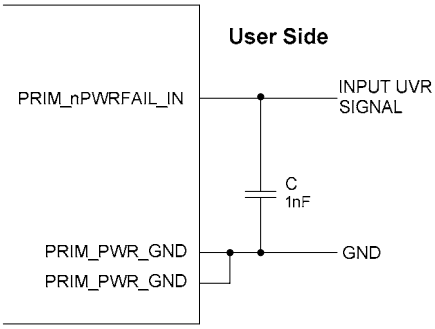
**Rising slope of the power supply voltage**




If the power supply is able to provide a higher current, a peak current will flow in the first instant to charge up the input capacitances on the driver. Its peak current value will be limited by the power supply and the effective impedances (e.g. distribution lines), only.
It is recommended to avoid the paralleling of several customer side power supply units. Their different set current limitations may lead to dips in the supply voltage.
The driver is ready for operation typically 150ms after turning on the supply voltage. The driver error signal PRIM_HOLD_OUT and PRIM_HOLD_IN are operational after this time. Without any error present, the PRIM_HOLD_OUT signal will be reset.
To assure a high level of system safety the TOP and BOT signal inputs should stay in a defined state (OFF state, LOW) during driver turn-on time. Only after the end of the power-on-reset, IGBT switching operation shall be permitted.

**Under Voltage Reset (UVR)**

The Under Voltage Reset circuit configures the driver core to hold in a reset state during power on and power off. UVR can be thought of as a supplement function to the build in power-on-reset by the user. While in reset, the driver is held in its initial condition until PRIM_nPWRFAIL_IN is forced into HIGH state. Once the system reset sequence completes, the driver core is ready to operate.

| UVR input | Application Hints |
|---|---|
|  | A capacitor is connected to the input to obtain high noise immunity.<br>**Disabling of the Under Voltage Reset function (PRIM_nPWRFAIL_IN) can be achieved by no connection or connection to +15V.** |

**Please note:**
Do not use PRIM_nPWRFAIL_IN to place the driver core into halt mode during operation.

**Under Voltage Protection (UVP) primary**

The internally detected supply voltage of the driver has an under voltage protection. The table below gives an overview of the trip level.

| Supply voltage | UVP level |
|---|---|
| Regulated +15V ±4% | 13,5V |

If the internally detected supply voltage of the driver falls below this level, the IGBTs will be switched off (IGBT driving signals set to LOW). The input side switching signals of the driver will be ignored. The error memory will be set, and the output PRIM_HOLD_OUT changes to the HIGH state.

**Under Voltage Protection secondary**

This function monitors the rectified voltage on the secondary side. If the voltage drops, the IGBTs will be switched off (IGBT driving signal set to LOW). The input side switching signals of the driver will be ignored. No failure message will be generated.

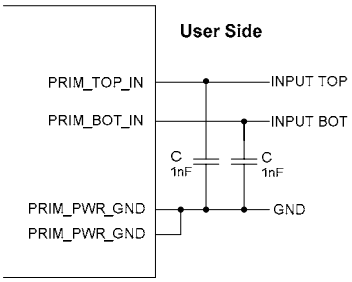
| Output voltage | UVP level |
|---|---|
| Regulated +15V | 12V |

**Input Signals**

The signal transfer to each IGBT is made with pulse transformers, used for switching on and switching off of the IGBT. The inputs have a Schmitt Trigger characteristic and a positive / active high logic (input HIGH = IGBT on; input LOW = IGBT off). It is mandatory to use circuits which switch active to +15V and 0V. Pull up and open collector output stages must not be used for TOP / BOT control signals. It is recommended choosing the line drivers according to the demanded length of the signal wires.

**Please note:**
It is not permitted to apply switching pulses shorter than 1µs.

**TOP / BOT Input**

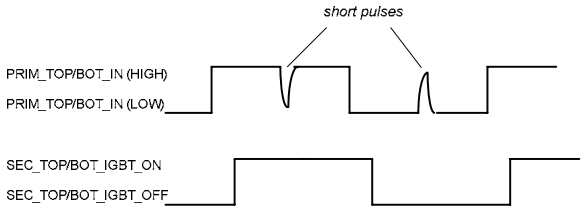



A capacitor is connected to the input to obtain high noise immunity. This capacitor can cause for current limited line drivers a little delay of few ns, which can be neglected. The capacitors have to be placed as close as possible to the driver interface.

### Short Pulse Suppression (SPS)

This circuit suppresses short turn-on and off-pulses of incoming signals. This way the IGBTs are protected against spurious noise as they can occur due to bursts on the signal lines. Pulses shorter than 625ns are suppressed and all pulses longer than 750ns get through for 100% probability. Pulses with a length in-between 625ns and 750ns can be either suppressed or get through.

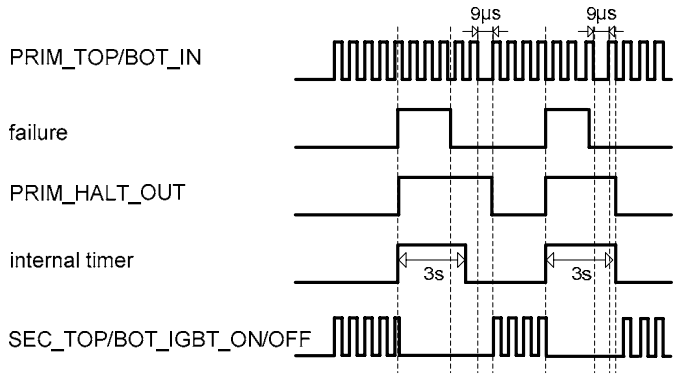
**Pulse pattern – SPS**




### Failure Management

A failure caused by PRIM_nPWRFAIL_IN, under voltage protection, dynamic short circuit detection or external error input will force PRIM_HALT_OUT into HIGH state (not ready to operate). The IGBTs will be switched off (IGBT driving signals set to LOW) and switching pulses from the controller will be not transferred to the output stage. Connected and switched off IGBTs remain turned off. At the same time an internal timer with a time constant of 3s is started. If no failure, caused by PRIM_nPWRFAIL_IN or under voltage protection is present anymore, a time of 3s after failure detection is passed and also TOP and BOT input signals are set to the LOW level for a period of minimum $t_{pERRRESET}$ > 9µs, the driver core is ready to operate and switching pulses are transferred to the output stage. If PRIM_HALT_OUT is HIGH state, the external error input is not monitored. A present failure signal at external error input during PRIM_HALT_OUT in HIGH state is again detected after a reset signal and first transfer of TOP and BOT switching pulses to the output stage.

**Pulse Pattern Failure Management**

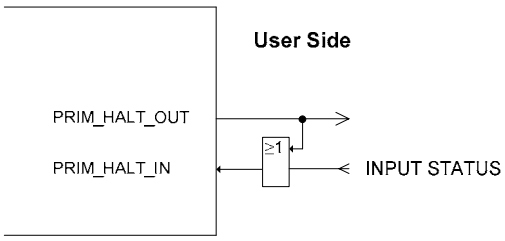
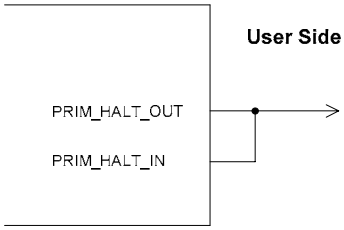



Propagation delay of the driver, interlock dead time and switching time of the IGBT chip has to be taken into account (not shown in the pulse pattern).

**Halt Logic Signal (HLS)**

The Halt Logic Signals PRIM_HALT_IN and PRIM_HALT_OUT show and control the drive core status. The driver core is placed into halt mode by setting PRIM_HALT_IN into HIGH state (disable driver). This signal can gather disable signals of other hardware components for stopping operation and switching off the IGBT. A HIGH signal will set the driver core into HOLD and switching pulses from the controller will be not transferred to the output stage. The input and output have Schmitt Trigger characteristic. Pull up and open collector output stages must not be used.

**Please note:**
PRIM_HALT_OUT must be always connected with PRIM_HALT_IN. PRIM_HALT_OUT is not short circuit proof.

| Connection PRIM_HALT_OUT and PRIM_HALT_IN | Connection PRIM_HALT_OUT (PRIM_HALT_IN not used) |
|---|---|
|  |  |



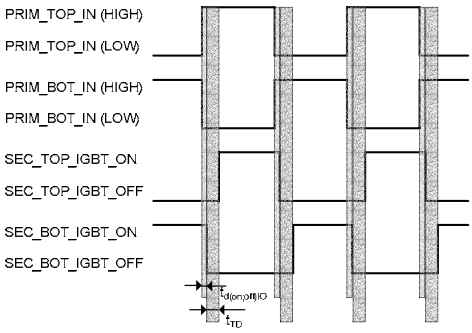


**Please note:**
A HIGH signal @ PRIM_HALT_IN does not generate a HIGH signal @ PRIM_HALT_OUT. After LOW signal @ PRIM_HALT_IN the gate driver is enable do operate.

**Dead Time generation (Interlock TOP / BOT) adjustable (DT)**

The DT circuit prevents, that TOP and BOT IGBT of one half bridge are switched on at the same time (shoot through). The dead time is not added to a dead time given by the controller. Thus the total dead time is the maximum of "built in dead time" and "controller dead time". It is possible to control the driver with one switching signal and its inverted signal.

**Pulse pattern – DT**




- The total propagation delay of the driver is the sum of interlock dead time ($t_{TD}$) and driver input output signal propagation delay ($t_{d(on;off)IO}$) as shown in the pulse pattern. Moreover the switching time of the IGBT chip has to be taken into account (not shown in the pulse pattern).
- In case both channel inputs (PRIM_TOP_IN and PRIM_BOT_IN) are at high level, the IGBTs will be turned off.
- If only one channel is switching, there will be no interlock dead time.

**Please note:**
No error message will be generated when overlap of switching signals occurs.

The dead time can be adjusted and the locking function may be neutralized as shown in the following table.

**Adjustment of Dead time / Neutralizing Locking Functions**

| Interlock time [µs] | PRIM_CFG_TDT1_IN | PRIM_CFG_TDT2_IN | PRIM_CDG_TDT3_IN | PRIM_CFG_SELECT_IN |
|---|---|---|---|---|
| 1 | GND | GND | open | open |
| 1,3 | GND | GND | GND | open |
| 2 | GND | open | open | open |
| 2,3 | GND | open | GND | open |
| 3 | open | GND | open | open |
| 3,3 | open | GND | GND | open |
| 4 * | open | open | open | open |
| 4,3 | open | open | GND | open |
| no interlock | open | open | open | GND |

*** Factory setting**

**Please note:**

The dead time has to be longer than the turn-off delay time of the IGBT in any case. This is to avoid that one IGBT is turned on before the other one is not completely discharged. If the dead time is too short, the heat generated by the short circuit current may destroy the module in the event of a short circuit in top or bottom arm.

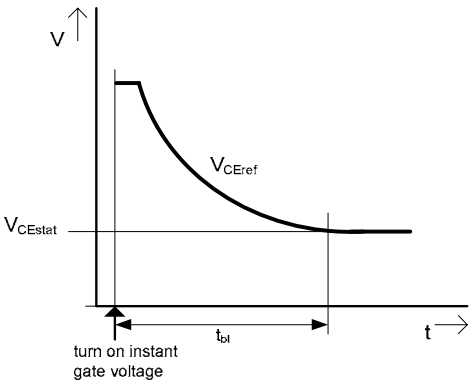
The average output current is available at each output channel. It is not possible to interconnect the output channels to achieve a higher average output current by neutralizing the locking function.

### Dynamic Short Circuit Protection by $V_{CEsat}$ monitoring / de-saturation monitoring (DSCP)

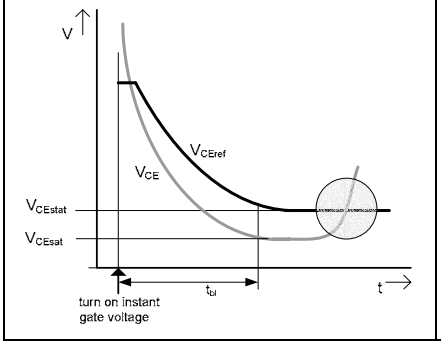
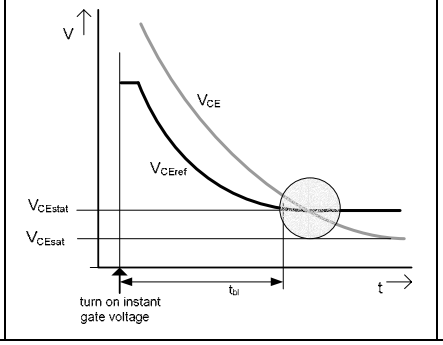
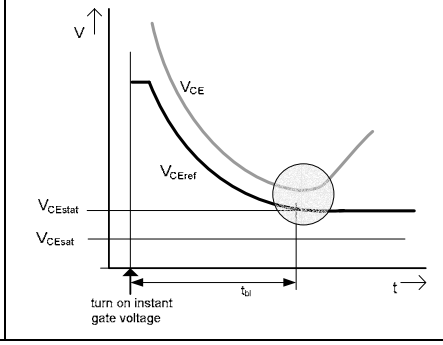
The DSCP circuit is responsible for short circuit sensing. It monitors the collector-emitter voltage $V_{CE}$ of the IGBT during its on-state. Due to the direct measurement of $V_{CEsat}$ on the IGBT's collector, the DSCP circuit switches off the IGBTs and an error is indicated.

The reference voltage $V_{CEref}$ may dynamically be adapted to the IGBTs switching behaviour. Immediately after turn-on of the IGBT, a higher value is effective than in steady state. This value will, however, be reset, when the IGBT is turned off. $V_{CEstat}$ is the steady-state value of $V_{CEref}$ and is adjusted to the required maximum value for each IGBT by an external resistor $R_{CE}$. It may not exceed 10V. The time constant for the delay (exponential shape) of $V_{CEref}$ may be controlled by an external capacitor $C_{CE}$, which is connected in parallel to $R_{CE}$. It controls the blanking time $t_{bl}$ which passes after turn-on of the IGBT before the $V_{CEsat}$ monitoring is activated. This makes an adaptation to any IGBT switching behaviour possible.

**Reference Voltage ($V_{CEref}$) Characteristic**




After $t_{bl}$ has passed, the $V_{CE}$ monitoring will be triggered as soon as $V_{CEsat} > V_{CEref}$ and will turn off the IGBT. The error memory will be set, and the output PRIM_HOLD_OUT changes to the HIGH state. Possible failure modes are shows in the following pictures.

| Short circuit during operation | Turn on of IGBT too slow * | Short circuit during turn on |
|---|---|---|
|  |  |  |

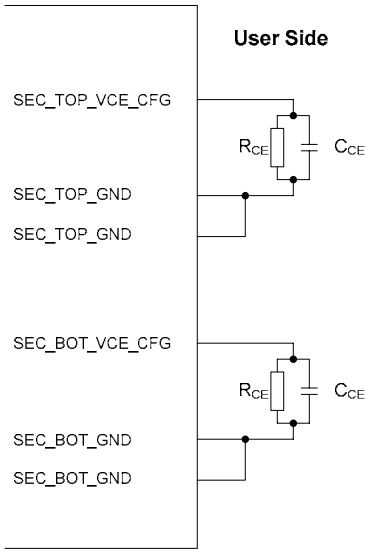


* or adjusted blanking time too short

**Adjustment of DSCP**

The external components $R_{CE}$ and $C_{CE}$ are applied for adjusting the steady-state threshold the blanking time.

**Connection $R_{CE}$ and $C_{CE}$**




**Dimensioning of $R_{CE}$ and $C_{CE}$**

$$R_{CE}[k\Omega] = -15{,}5k\Omega \cdot \ln\left(1 - \frac{V_{CEstat} + R_{VCE} \cdot \frac{V}{k\Omega}}{8V}\right)$$

$$C_{CE}[pF] = \frac{t_{bl}[\mu s] - 2{,}1\mu s - 0{,}11\frac{\mu s}{\Omega} \cdot R_{CE}}{0{,}00323\frac{\mu s}{pF}}$$

$V_{CEstat}$: Collector-emitter threshold static monitoring voltage
$t_{blx}$: Blanking time

$V_{CEstat\_max}$ = 8V ($R_{VCE}$ = 0Ω)
$V_{CEstat\_max}$ = 7V ($R_{VCE}$ = 1kΩ)

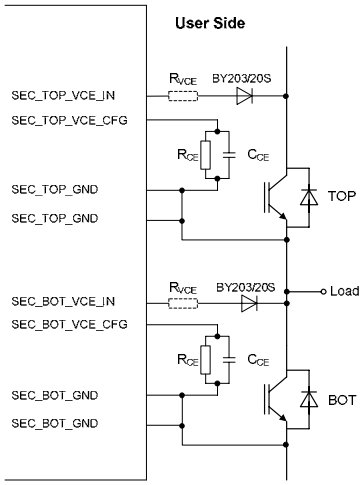
**Please Note:**
The equations are calculated considering the use of high voltage diode BY203/20S. The calculated values $V_{CEstat}$ and $t_{bl}$ are typical values at room temperature can and do vary in the application (e.g. tolerances of used high voltage diode, resistor $R_{CE}$, capacitor $C_{CE}$).
The DSCP function is not recommended for over current protection.

**Application hints**

If the DSCP function is not used, for example during the experimental phase, SEC_TOP_VCE_IN must be connected with SEC_TOP_GND for disabling SCP @ TOP side and SEC_BOT_VCE_IN must be connected with SEC_BOT_GND for disabling SCP @ BOT side.

### High Voltage Diode for DSCP

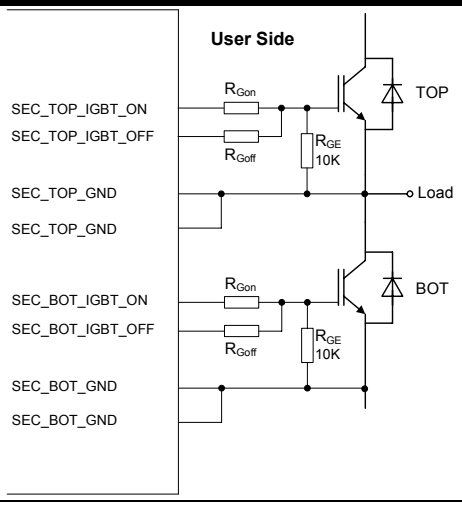
The high voltage diode blocks the high voltage during IGBT off state. The connection of this diode between driver and IGBT is shows in the following schematic.

| Connection High Voltage Diode | Characteristics |
|---|---|
|  | ▪ Reverse blocking voltage of the diode shall be higher than the used IGBT.<br>▪ Reverse recovery time of the fast diode shall be lower than $V_{CE}$ rising of the used IGBT.<br>▪ Forward voltage of the diode: 1,5V @ 2mA forward current ($T_j$=25°C).<br>**A collector series resistance $R_{VCE}$ (1kΩ / 0,4W) must be connected for 1700V IGBT operation.** |



### Gate resistors

The output transistors of the driver are MOSFETs. The sources of the MOSFETs are separately connected to external terminals in order to provide setting of the turn-on and turn-off speed of each IGBT by the external resistors $R_{Gon}$ and $R_{Goff}$. As an IGBT has input capacitance (varying during switching time) which must be charged and discharged, both resistors will dictate what time must be taken to do this. The final value of the resistance is difficult to predict, because it depends on many parameters as DC link voltage, stray inductance of the circuit, switching frequency and type of IGBT.

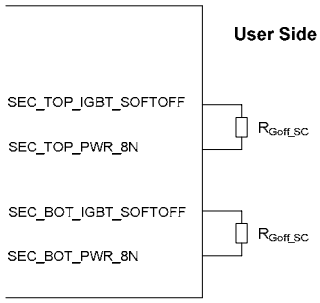
| Connection $R_{Gon}$, $R_{Goff}$ | Application Hints |
|---|---|
|  | The gate resistor influences the switching time, switching losses, dv/dt behaviour, etc. and has to be selected very carefully. Due to this influence a general value for the gate resistors cannot be recommended. The gate resistor has to be optimized according to switching behaviour and over voltage peaks within the specific circuitry.<br>By increasing $R_{Gon}$ the turn-on speed will decrease. The reverse peak current of the free-wheeling diode will diminish.<br>By increasing $R_{Goff}$ the turn-off speed of the IGBT will decrease. The inductive peak over voltage during turn-off will diminish.<br>In order to ensure locking of the IGBT even when the driver supply voltage is turned off, a resistance ($R_{GE}$) has to be integrated. |



**Please note:**
Do not connect the terminals SEC_TOP_IGBT_ON with SEC_TOP_IGBT_OFF and SEC_BOT_IGBT_ON with SEC_BOT_IGBT_OFF, respectively.

### Soft Turn-Off (STO)

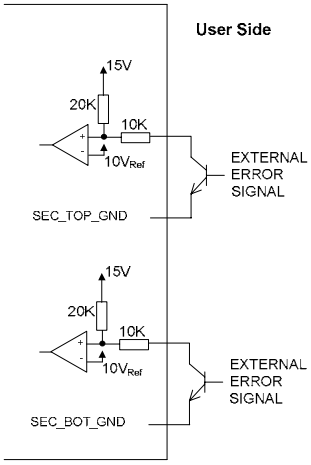
In case of short circuit, the STO circuit increases the resistance in series with $R_{Goff}$ and turns-off the IGBT at lower speed. This produces smaller voltage spike above the collector emitter of the IGBT by reducing the di/dt value. Because in short-circuit conditions the IGBT's peak current increases and some stray inductance is always present in power circuits, it must fall to zero in a longer time than at normal operation. The soft turn-off time can be adjusted by connection an external resistor $R_{Goff\_SC}$.

| Connection $R_{Goff\_SC}$ | Application Hints |
|---|---|
|  | The turn-off behaviour and over voltage peaks depends on DC link voltage, stray inductance of the power circuits, type of IGBT, etc. and has to be selected according the specific application. Due to this influence a general value for $R_{Goff\_SC}$ cannot be recommended. The resistor has to be selected according to the behaviour of the specific circuitry.<br><br>The soft turn-off time is limited to 10µs. After this time the output stage turn-off with used $R_{Goff}$.<br><br>Disabling of Soft Turn-Off can be achieved by $R_{Goff\_SC}$ = 0Ω or wire bridge. |

**Please note:**
The soft turn-off function is no complete protection from induced over voltage in the event of short-circuit turn-off.
A HIGH signal at PRIM_HALT_IN does not activate a soft turn-off.

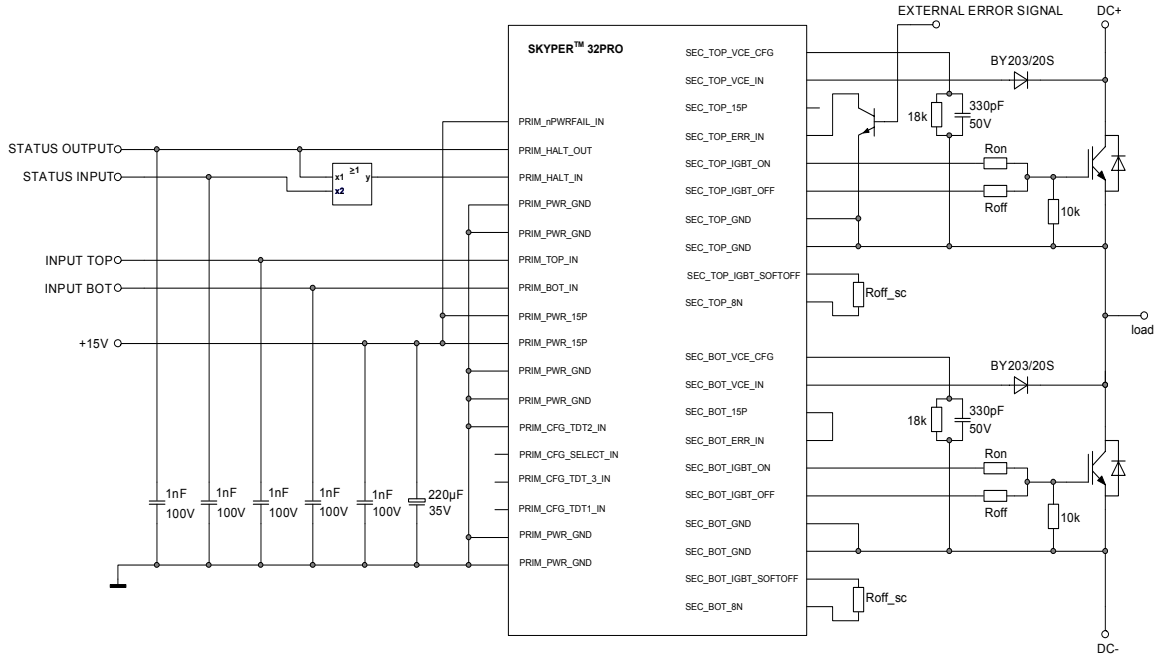
### External Error Input (EEI)

The external error inputs on the secondary side (high potential) of the gate driver can be used for external fault signals from e. g. an over current protection circuit or over temperature protection circuit to place the gate driver into halt mode.
Disabling of this function can be achieved by no connection or connection to +15V (e. g. SEC_TOP_15P, SEC_BOT_15P to SEC_TOP_ERR_IN and SEC_BOT_ERR_IN). It is possible to use only one error input.

| Connection EEI | |
|---|---|
|  | Connection example with using an external transistor in switch mode. |

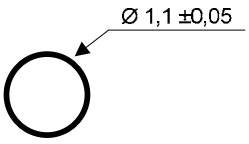
## Application Example

**Connection Schematic**



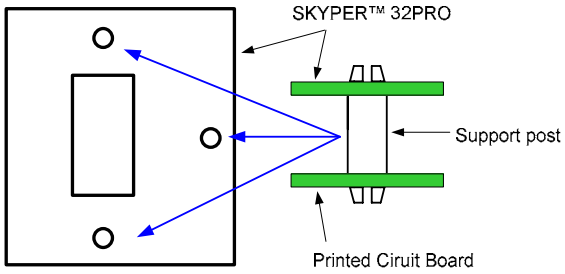

- application example for 1200V IGBT
- dead time: 3µs
- UVR disable
- $V_{CEref}$ = 5,5V
- $t_{bl}$ = 5,1µs
- EEI TOP enable (using external transistor in switch mode)
- EEI BOT disable
- STO

## Mounting Notes

| Soldering Hints | Drill Hole & Pad Size in mm |
|---|---|
| The temperature of the solder must not exceed 260°C, and solder time must not exceed 10 seconds.<br><br>The ambient temperature must not exceed the specified maximum storage temperature of the driver.<br><br>The solder joints should be in accordance to IPC A 610 Revision D (or later) - Class 3 (Acceptability of Electronic Assemblies) to ensure an optimal connection between driver core and printed circuit board. |  <br>pad size: min. 1,8 |

**Please note:**
The driver is not suited for hot air reflow or infrared reflow processes.

The connection between driver core and printed circuit board should be mechanical reinforced by using support posts.

| Use of Support Posts | |
|---|---|
|  | Product information of suitable support posts and distributor contact information is available at e.g. http://www.richco-inc.com (e.g. series DLMSPM, LCBST). |

**Please note:**
The use of agressive materials in cleaning process of driver core may be detrimental for the device parameters.

### Environmental Conditions

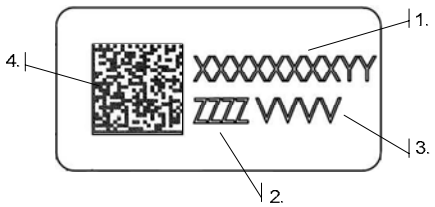
The driver core is type tested under the environmental conditions below.

| Conditions | Values (max.) |
|---|---|
| Vibration | Sinusoidal sweep 20Hz … 500Hz, 5g, 26 sweeps per axis (x, y, z)<br>- Tested acc. IEC 68-2-6<br>- Connection between driver core and printed circuit board mechanical reinforced by using support posts. |
| Shock | Half-sinusoidal pulse, 5g, shock width 18ms, 3 shocks in each direction (±x, ±y, ±z), 18 shocks in total<br>- Tested acc. IEC 68-2-27<br>- Connection between driver core and printed circuit board mechanical reinforced by using support posts. |

The characteristics and further environmental conditions are indicated in the data sheet.

**Marking**

Every driver core is marked. The marking contains the following items.

| Part Marking Information | |
|---|---|
|  <br>1. SEMIKRON part number (8 digits) + version number (2 digits)<br>2. Date code (4 digits): YYWW<br>3. Continuous number referred to date coce (4 digits)<br>4. Data matrix code | The Data Matrix Code is described as follows:<br>▪ Type: EEC 200<br>▪ Standard: ICO / IEC 16022<br>▪ Cell size: 0,254 - 0,3 mm<br>▪ Dimension: 5 × 5 mm<br>▪ The following data is coded:<br>❶ ❷ ❸ ❹ ❺<br>XXXXXXXXYY ZZZZ VVVV<br>❶ 8 digits part number<br>2 digits version number<br>❷ 1 digit blank<br>❸ 4 digits date code<br>❹ 1 digit blank<br>❺ 4 digits continuous number |



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